Chittagong University of Engineering and Technology

Department of Electrical and Electrical Engineering

EEE 490: VLSI Technology Sessional

Project No. # 3

Project Name:A Comparator for 2 n-bit number.Designing cascadable comparator cell and cascade it to form a comparator for two 4-bit numbers

Prepared By

Student Name: M A HAFIZ
Student ID: 1302044
Group No.: 13
Student IDs of Group Members: 1302044,1302056
Section: A_2
Date of Report: July 9, 2018

ABSTRACT

The goal of this project is to design a two n-bit comparator, aiming to design cascadable comparator cell and cascade it to form a comparator for 2 4-bit numbers.The details of designing a 4-bit comparator are given in this report. It involves the methodology, circuit implementation, schematic simulation, layout,LVS, DRC Error Check.

We start from logic gate level, go up to the circuit level and then draw the layout in Layout window of Cadenece. Finally we extract the layout as a symbol in the schematic for re-simulation to obtain the results of the performance measure. In designing, propagation delay, Area (A) and power are considered. All parameters of circuit are decided and the circuit plot and waveform are produced, and we would test and verify every part of the CMOS circuit developed by Cadence development tools . The test results from simulation can meet the requirement. It means that the logic design, schematic and layout are correct, and our project can satisfy the requirements.

KEYWORDS

1. Cadence
2. NAND
3. DRC
4. XNOR
5. Virtuoso
6. LVS
7. Inverter

Table of Contents

List of Figures

1 Introduction

1.1 Description of this project

The goal is the design of a 4-bit comparator. Input two 4-bit numbers A & B. Output is 3-bit (A¡B, A¿B and A=B). We may use any comparison form and any logic form static, dynamic, or any variation of these or within these families.

1.2 Schematic Design

Perform schematic design for every blog of comparator cirtuit.The schematic of XNOR,NAND,Inverter and other blocks are designed before completing the full schematic design of comparator circuit. Then by adding each block to another, the whole schematic comparator circuit is designed.

1.3 Symbol

For every part of comparator circuit, symbol is created with pin connection. Then the simulation of every part is performed to testify that whether they are providing correct output or not.Then combining all blocks the logic circuit is designed for comparator.

1.4 Layout

Layout for every part is designed and the whole layout is designed. After layout design, the simulation is performed and checked the output waveform to evaluate the comparator operation.

1.5 LVS and DRC

Finally, to justify the project output, LVS is checked to match layout and schematic. After matching layout and schematic, the wiring connection is checked using DRC. When the DRC error is come down to zero, only then the goal of this project is satisfied.

2 Methodology

2.1 Design Procedure

Magnitude comparator is a combinational circuit that compares to numbers and determines their relative magnitude. A comparator is shown as figure 2.1. The output of comparator is usually 3 binary variables indicating:

$$A > B$$
$$A = B$$
$$A < B$$

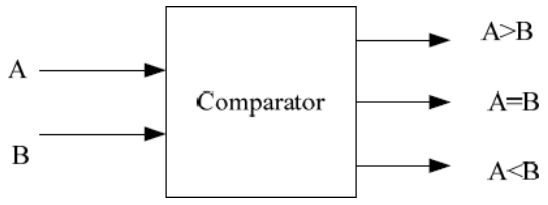

Figure 1: 1-bit Comparator

2.2 4-bit comparator

The procedure for binary numbers with more than 2 bits can be found in the following way. The figure 2 shows the 4-bit magnitude comparator.

Input A=A3A2A1A0; B=B3B2B1B0

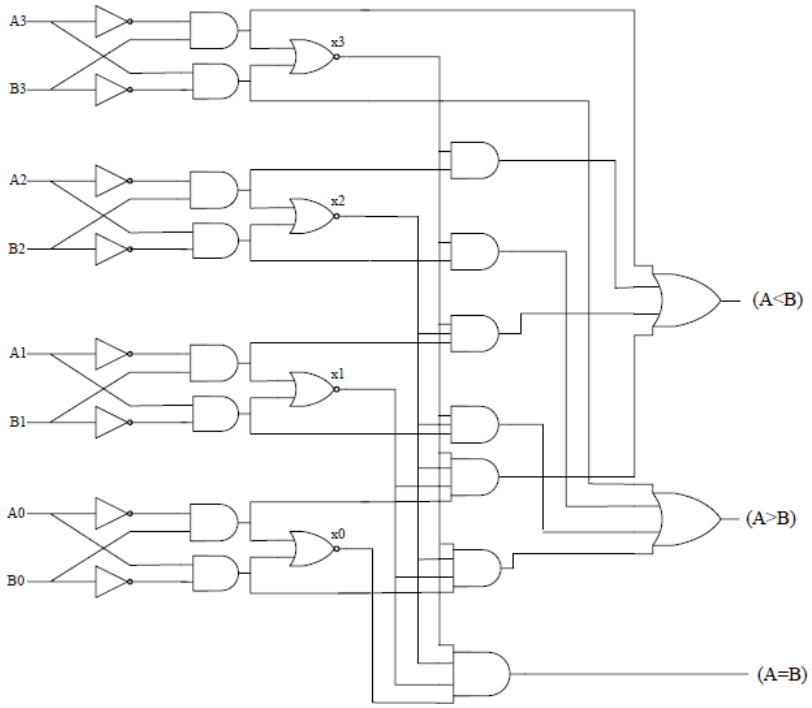

Figure 2: 4-bit Magnitude Comparator

(1) A= B : A3=B3, A2=B2, A1=B1, A0=B0
xi = Ai*Bi + Ai'Bi'
XOR-Invert =(AiBi' + Ai'Bi)
=(Ai' + Bi)(Ai+Bi')
=Ai'Ai + Ai'Bi' + AiBi + BiBi'
=AiBi + Ai'Bi'

Output: x3x2x1x0

(2) A>B
Output: A3B3'+ x3A2B2' + x3x2A1B1'+ x3x2x1A0B0'

(3)(A< B)
Output: A'3B3 + x3A'2B2 + x3x2A'1B1+ x3x2x1A'0B0
In order to reduce the area, we can still decrease the number

COMPARING INPUTS				OUTPUT		
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**A > B**	**A < B**	**A = B**
A3 > B3	X	X	X	H	L	L
A3 < B3	X	X	X	L	H	L
A3 = B3	A2 >B2	X	X	H	L	L
A3 = B3	A2 < B2	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H
H = High Voltage Level, L = Low Voltage, Level, X = Don't Care						

Figure 3: Truth Table of 4-bit Comparator

of gates. The logic of A¡B can be decided by A¿B and A=B, so we can simplify the above circuit as figure2.2-input NOR is used here to realize the function of A¡B. The area of 2-input NOR is much less than that of G11 G15. On the other hand, fewer gates means fewer power, so this modification can greatly reduce the power dissipation. Therefore, the logic optimization is completed.

In order to verify above design, we start to do logic simulation.

3 Procedure

From the simplified logic diagram, we can see that the circuit include 4 XOR gates, 5 AND gates with inputs from 2 to 5, 4 inputs and 2 inputs NOR and 5 inverters. In designing, we select the time and the area as performance index for optimization. Although area is an advantage for pseudo-Nmos, we will not adopt it after entirely thinking about td, tphl, tplh, area, power dissipation and other performance parameters.we can see that a 4 input NOR is used in the circuit. As we know, NOR gates are costly. For the same performance, it results in increased area, power, delay, output load capacitance (due to an increase in drain diffusion capacitance) and increase in input capacitance presenting higher load to driver circuit. Normally we convert our circuit to NAND and avoid use of large fan in NOR. But in this project, we still choose 2 inputs NOR as for practice since its fan-in is only 2, and measure the performance to get the detailed data with which we can compare the characteristics.Here we display four parts of comparator schematic: XNOR, NOR, Inverter, NAND and measure it after simulation.

3.1 XNOR Circuit Design and Simulation

XNOR schematic diagram is given below.

This simulation is performed in the Command Interpreter Window of Virtuoso Cadence Software.The layout and simulation waveform are given below.

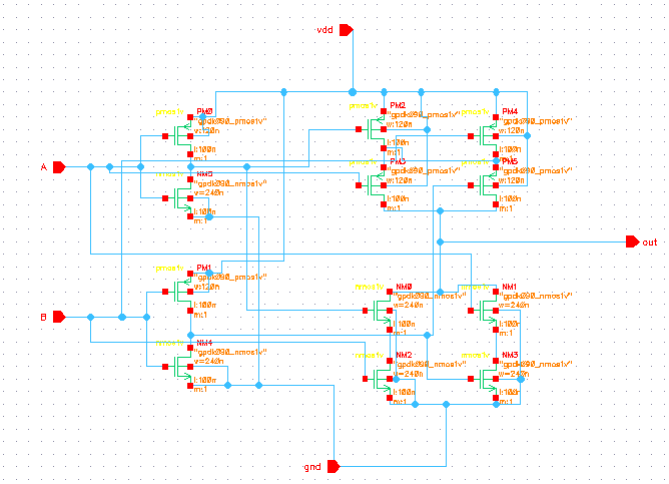

Figure 4: Schematic Diagram of 2-input XNOR

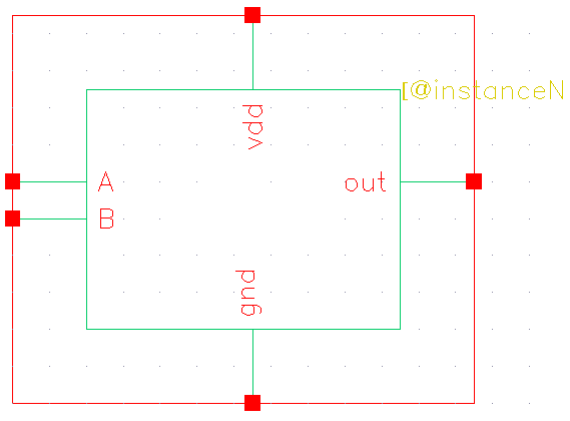

Figure 5: Symbol of XNOR

Figure 6: Output Waveform of 2-input XNOR

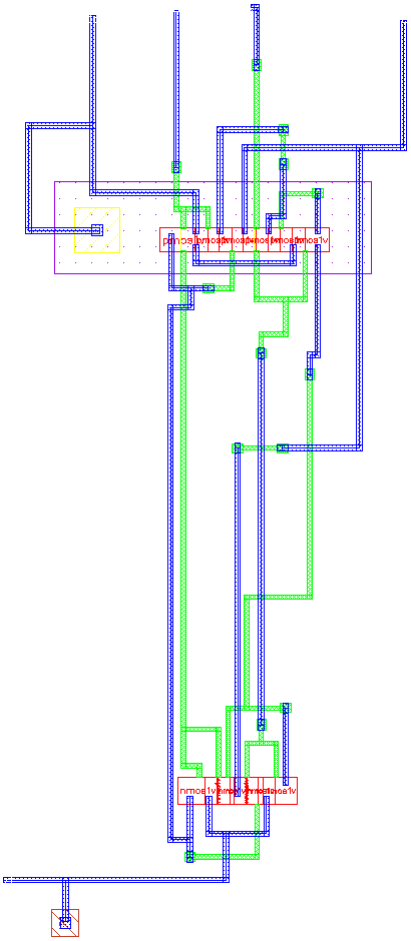

Figure 7: layout diagram of XNOR

3.2 NOR Circuit Design and Simulation

A schematic of 4-input NOR circuit is given below.

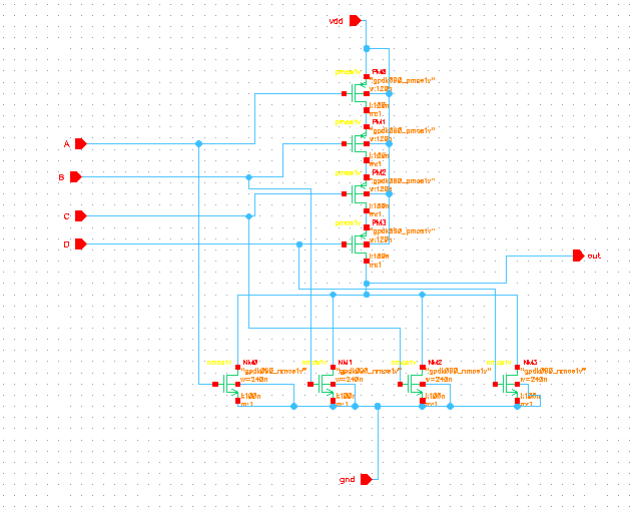

Figure 8: Schematic diagram of NOR

Symbol,Schematic simulation and layout of NOR gate are given below.

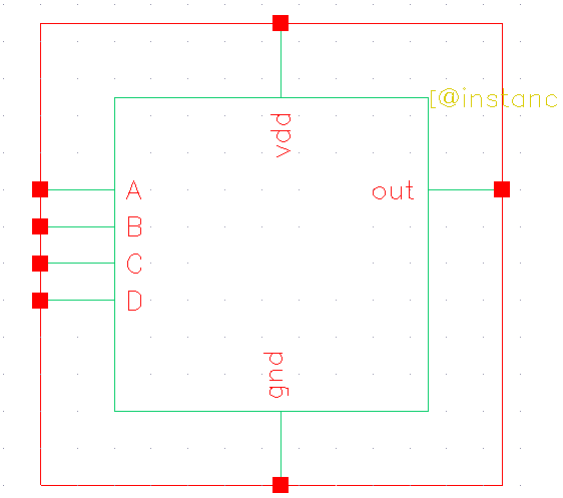

Figure 9: Symbol of NOR

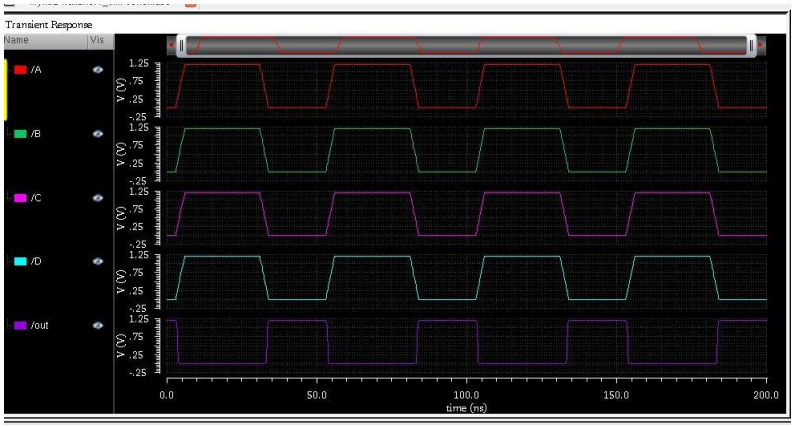

Figure 10: Output Waveform of NOR

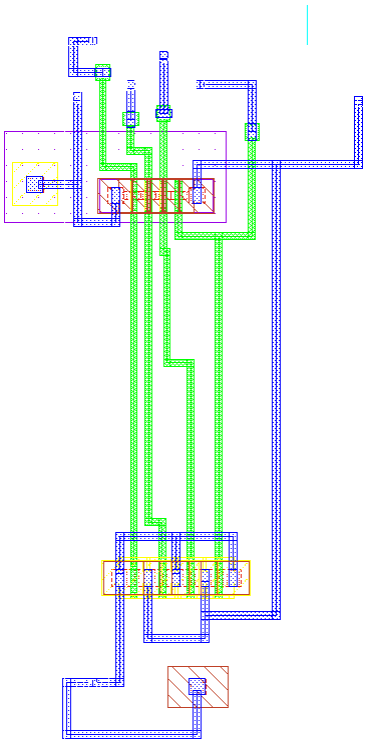

Figure 11: layout diagram of NOR

3.3 NAND Circuit Design and Simulation

NAND gate of different input are used here to complete comparator design. Among of them, a 4-input NAND schematic is given below.

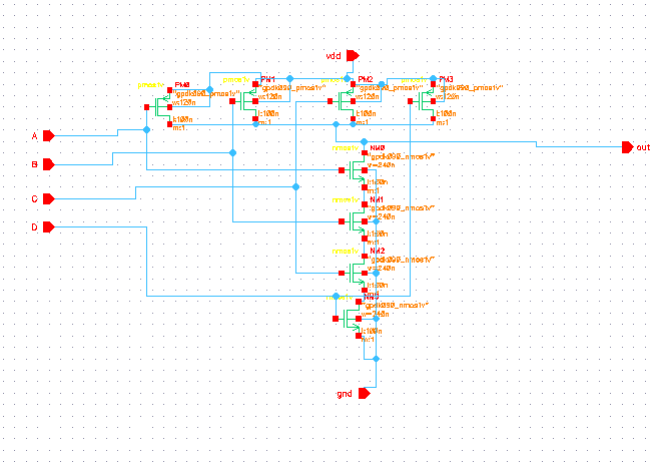

Figure 12: Schematic diagram of NAND

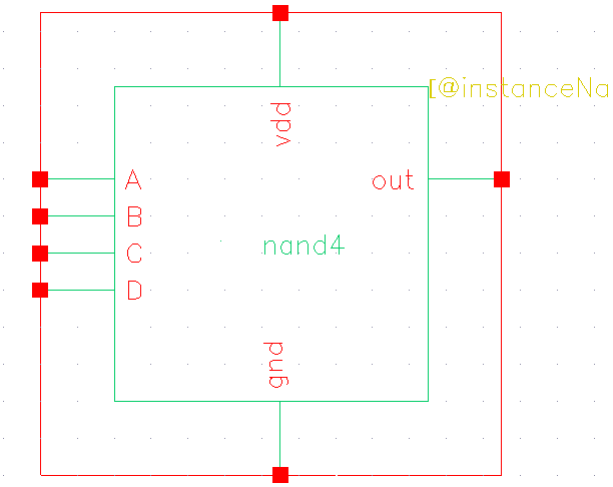

Figure 13: Symbol of NAND

Figure 14: Output waveform of NAND

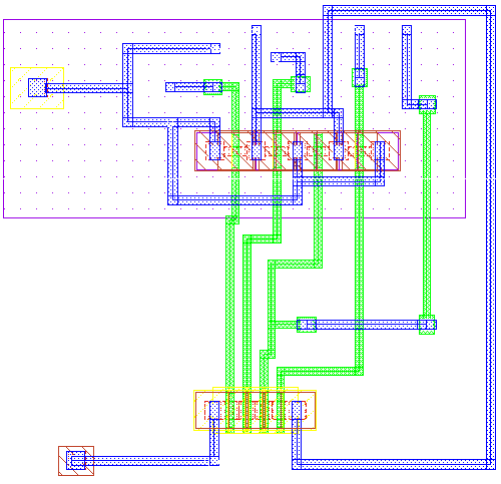

Figure 15: layout diagram of NAND

3.4 Inverter Circuit Design and Simulation

Schematic ,symbol,simulation waveform and layout of inverter is given as follow:

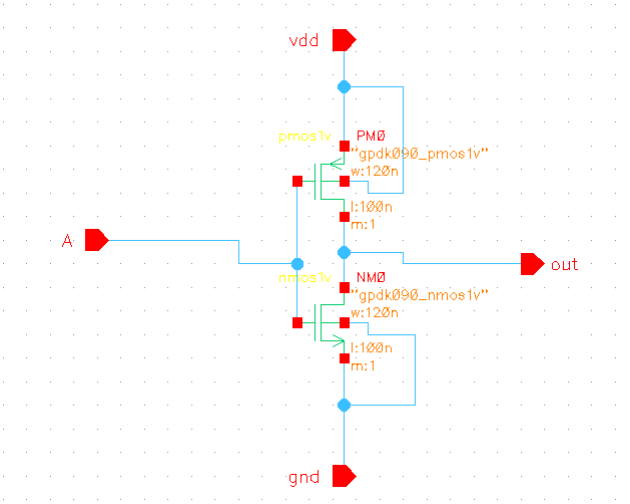

Figure 16: Schematic Diagram of Inverter

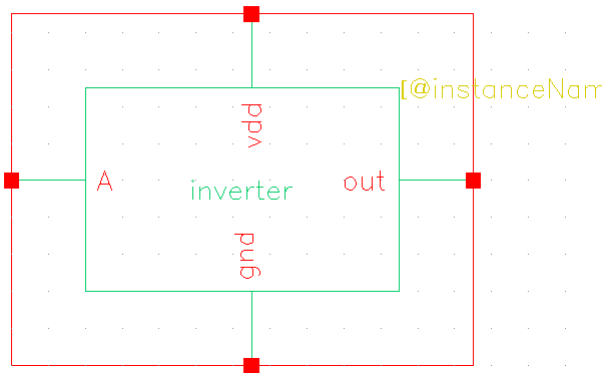

Figure 17: Symbol of Inverter

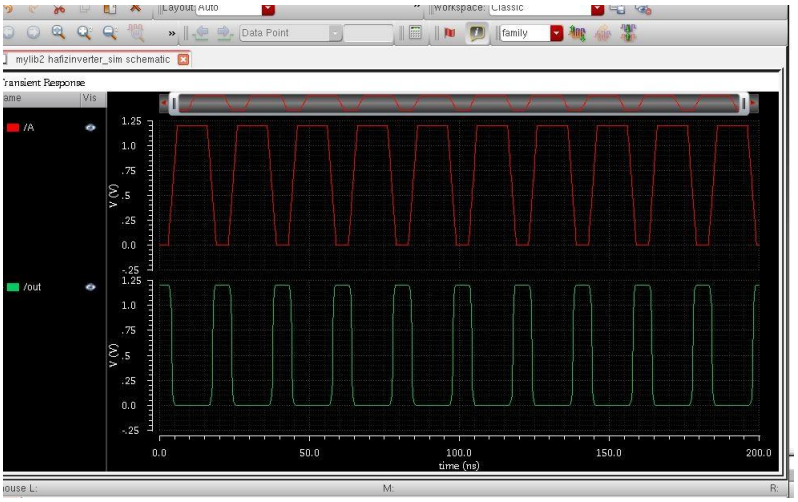

Figure 18: Simulation Waveform of Inverter

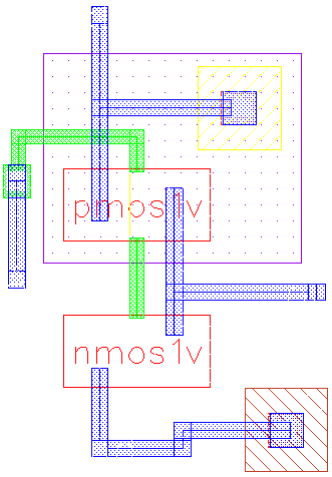

Figure 19: Layout Diagram of Inverter

4 Final Circuit Design and Simulation

Finally after checking output of all blocks of comparator, they are combined to create the main schematic design of 4-bit comparator.The schematic diagram,simulation result,layout, LVS and DRC is given below.

4.1 Schematic of Full Comparator

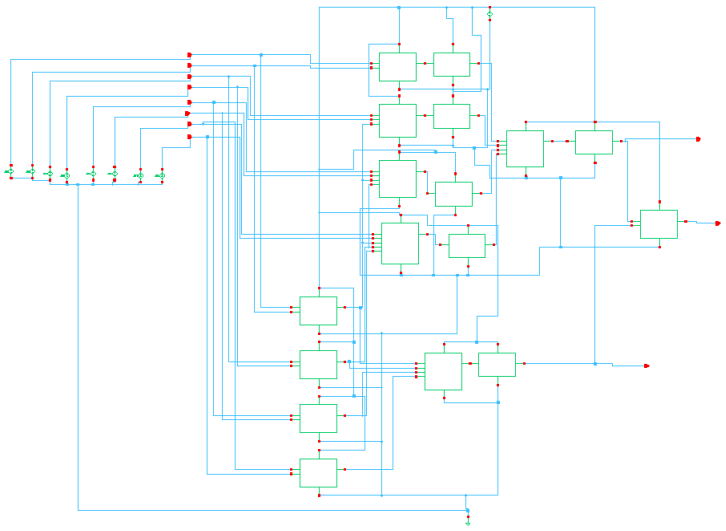

Figure 20: Total Schematic Design of Comparator

4.2 Simulation

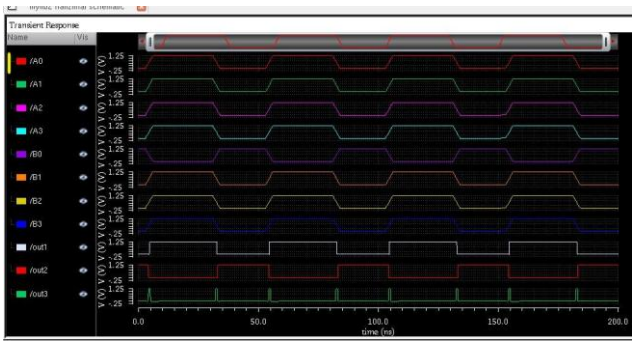

Figure 21: Simulation Waveform of Comparator

4.3 Layout,LVS,DRC Check

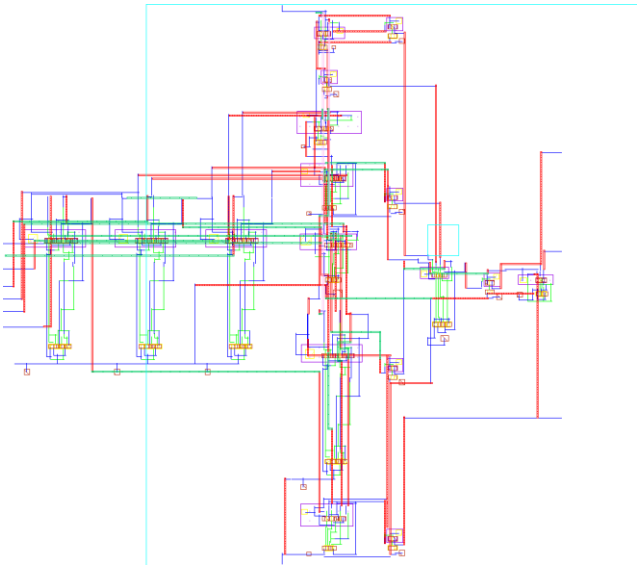

Figure 22: Layout Diagram of Comparator

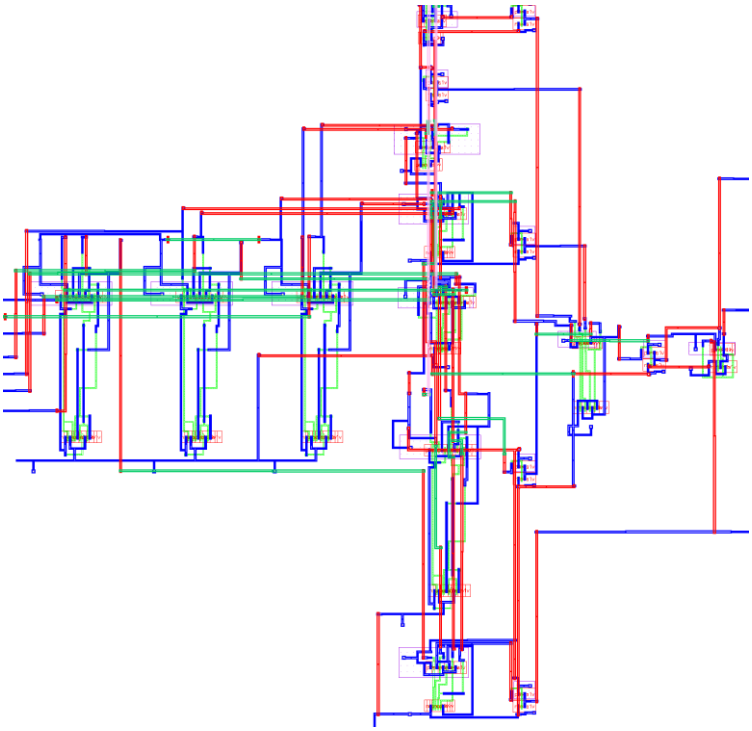

Figure 23: Layout Diagram of Comparator for Parasaitic Capacitance

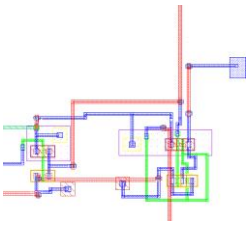

Figure 24: Layout Diagram of Comparator for tapped pin

After completing final layout of comparator for different conditions, the LVS and DRC are completed to justify the accuracy of this design.

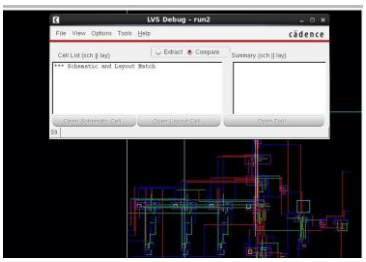

Figure 25: LVS Check for Comparator Design

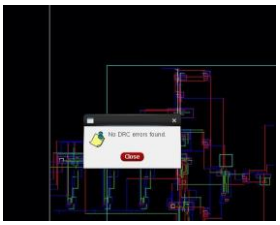

Figure 26: DRC Error of Comparator Simulation

5 Verilog Code and Circuit Simulation of Comparator

After completing schematic and layout simulation, now the comparator circuit condition is created by verilog code. After inputting verilog code in text window, the created circuit is observed and hence from the circuit, the output waveform is justified whether the circuit satisfies the condition of comparator.

5.1 Verilog Code

4 bit Comparator:

```
//declare the Verilog module - The inputs and output signals.
module comparator (
Data_in_A , //input A
Data_in_B , //input B
less ,
//high when A is less than B
equal,
//high when A is equal to B
greater
//high when A is greater than B
) ;
//what are the input ports.
input [ 3 : 0 ] Data_in_A ;
input [ 3 : 0 ] Data_in_B ;
//What are the output ports.
output less ;
output equal ;
output greater ;
//Internal variables
```

```
reg less ;
reg equal ;
reg greater ;
//When the inputs and A or B are changed execute this block
always @ ( Data in A or Data in B )
begin
if (Data_in_A ¿ Data in B )
begin
//check if A is bigger than B.
less = 0;
equal = 0 ;
greater = 1 ; end
else if ( Data_in_A ==
Data_in_B ) begin
//Check if A is equal to B
less = 0;
equal = 1 ;
greater = 0 ; end
else begin
//Otherwise - check for A less than B.
less = 1;
equal = 0 ;
greater = 0 ;
end
end
endmodule
```

Testbench for Comparator:

```
module tb_tm ;
// Inputs
reg [ 3: 0 ] Data in A ;
reg [ 3: 0 ] Data_in_B ;
```

```
// Outputs
wire less ;
wire equal ;
wire greater ;
// Instantiate the Unit Under Test (UUT)
comparator uut (
.Data_in_A ( Data_in_A ),
.Data_in_B ( Data_in_B ),
.less ( less ),
.equal ( equal) ,
.greater ( greater)
) ;
initial  begin
//Apply inputs
Data_in_A = 10 ;
Data_in_B = 12 ;
# 100;
Data_in_A = 15 ;
Data_in_B = 11 ;
# 100;
Data_in_A = 10 ;
Data_in_B = 10 ;
# 100;
end
endmodule
```

5.2 Programming Window and Simulation Waveform

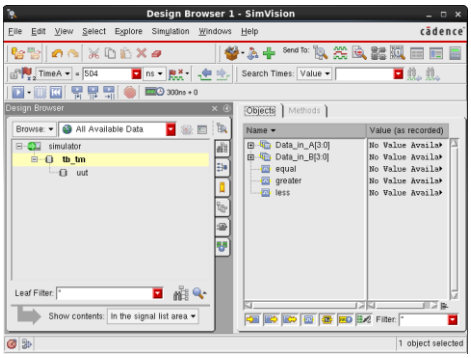

Figure 27: SimVision window of Verilog programme

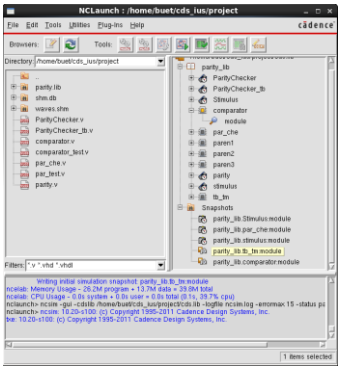

Figure 28: NCLaunch Window of Verilog

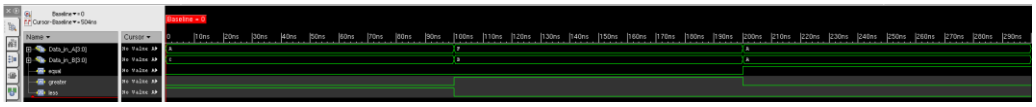

Figure 29: Output Waveform Created By Verilog

6 Conclusion

From the schematic level design and simulation, layout, verilog code and it's simulation waveform, it is clear that the logic of comparator is correct and simple to implement. According to the basic principles of CMOS circuit design, the appropriate parameters can be decided after several attempts to get better performance during the course of the circuit schematic design.The difference between the results from circuit design simulation and

layout simulation provides us specific clues for improving the layout and at the same time, we must see that the schematic is closer to layout and the output waveform of verilog is also similar to schematic output. For the practical application, some effects will be unavoidable, which is different from the circuit design simulation.